Remarks/Arguments

Claims 1-10, 12-20 and 23-25 remain in this application.

Claims 11, 21 and 22 have been cancelled.

The examiner has rejected claim 15 under 35 U.S.C. 102(e) as being anticipated by *Zimmer, et al.* (U.S. Patent Application Publication No. 2004/0103272).

The examiner has rejected claims 1-4, 6, 8 and 12-13 under 35 U.S.C. 103(a) as being unpatentable over *Lee* (U.S. Patent Application Publication No. 2005/0086464) in view of *Bernhard, et al.* (U.S. Patent Application Publication No. 2003/0233534).

The examiner has rejected claims 5, 9 and 10 under U.S.C. 103(a) as being unpatentable over the combination of *Lee* and *Bernhard, et al.* and further in view of *Zimmer, et al.*

The examiner has allowed claims 14, 16-20 and 23-25.

The examiner has objected to claim 7 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In view of the previous amendments and these remarks, reconsideration of the above noted rejections and objections is respectfully requested.

Rejection under 35 USC 102(e):

Applicant respectfully traverses the rejection of **claims 15** under 35 U.S.C. 102(e) as being anticipated by *Zimmer, et al.* **Claim 15** recites (among other limitations):

> under control of the stackless instructions the computer system initializes the **first computer memory** for **use by** the **memory controller**; and
> under control of the stack-based instructions the computer system assembles configuration data which **enables the memory controller to use the first and second computer memory**.

Applicant respectfully submits that *Zimmer, et al.* does not teach or suggest these limitations.

The office action equates the cache 14 and the interface 22 of *Zimmer, et al.* with the claimed first computer memory and the memory controller, respectively. However, *Zimmer, et al.* appears not to teach or suggest that the interface 22 **uses** the cache 14. As pointed out in the office action, the cache 14 is initialized **in the processor** 10. Since the cache 14 is in the processor 10, it is the **processor** 10, **not the interface** 22, that **uses** the cache 14. (See [0010] and [0012].) Then, after the cache 14 is initialized for **use by the processor** 10, the system memory 25 is initialized (see [0019]), presumably so that the system memory 25 can be used by the interface 22. (See also Fig. 2.) Applicant respectfully submits, therefore, that independent **claim 15** is not anticipated by, is not obvious in view of, and is patentable over *Zimmer, et al.* at least because the reference does not teach or fairly suggest 1) a memory controller that is initialized to **use a first computer memory** under control of stackless instructions and 2) configuration data, assembled under control of stack-based instructions, which enables the memory controller to **use BOTH first and second computer memory**.

Rejections under 35 USC 103(a):

Applicant respectfully traverses the rejection of **claims 1-4, 6, 8 and 12-13** under 35 U.S.C. 103(a) as being unpatentable over *Lee* in view of *Bernhard, et al.* and the rejection of **claims 5, 9 and 10** under 35 U.S.C. 103(a) as being unpatentable over *Lee* and *Bernhard, et al.* and further in view of *Zimmer, et al.* Attached to this document is a **Declaration under 37 C.F.R. § 1.131** signed by the sole inventor, David L. Collins, of the claims in this patent application. David L. Collins declares that attached to the Declaration is a flowchart that was prepared by him or under his direct supervision. Also, all work and associated writings were carried out in the United States. Additionally, all dates on the attached exhibits have been masked unless otherwise stated herein by reference to specific dates. David L. Collins further declares that prior to October 16, 2003, the effective date of *Lee*, he completed his invention as described and claimed in this application, as evidenced by the following:

According to the procedure shown in the attached flowchart, I
prepared a test program that upon reset of a computer (i.e. starting
computer memory initialization) 1). determined whether the reset was
firmware initiated. If the reset was NOT firmware initiated, then 2).
stackless memory initialization code was executed to initialize a first
memory controller and a portion of memory associated with this
controller, 3). a software stack and variables were then initialized, 4).
using the stack and variables, full stack-based memory initialization
code was executed for the first memory controller to use the full
memory associated with this controller, 5). formatted memory controller
configuration data was thus generated for the first memory controller
and its associated memory, and the data was saved in an EEPROM of
a memory module, and 6). a "firmware reset" flag was then set and a
"reset" was executed. Following the reset of the computer after
performance of the above portion of this procedure (i.e. upon restarting
the computer memory initialization), this procedure then 7). determined
that the reset was firmware initiated, so 8). the saved formatted
configuration data was copied from the memory module EEPROM to
the first memory controller using stackless instructions, and 9). a stack
and variables were then initialized so that stack-based full memory
initialization code was executed for the remaining memory controllers
and their associated memory.

Applicant respectfully submits, therefore, that David L. Collins' **Declaration
under 37 C.F.R. § 1.131** establishes invention of the subject matter of the rejected
claims prior to the effective date of *Lee*. In consequence, Applicant respectfully
requests that the rejections under 35 U.S.C. 103(a) incorporating *Lee* be withdrawn.

Allowed and Allowable Claims:

Applicant thanks the Examiner for allowing **claims 14, 16-20 and 23-25**.
Applicant thanks the Examiner for indicating that **claim 7** would be allowable if
rewritten. **Claim 7** has not been amended, since its base claim 1 (and intervening
claim 6) are patentable over the cited references, as explained above.

Conclusion:

For the reasons specifically discussed above, and others, it is believed that
pending **claims 1-10, 12-20 and 23-25** define patentable subject matter.
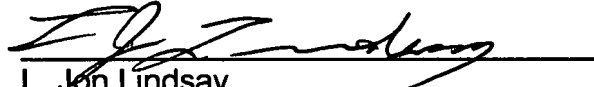Reconsideration of the previous rejections and objections as they might apply to the

pending claims is therefore respectfully requested. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

<u>August 17, 2007</u>
Date

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